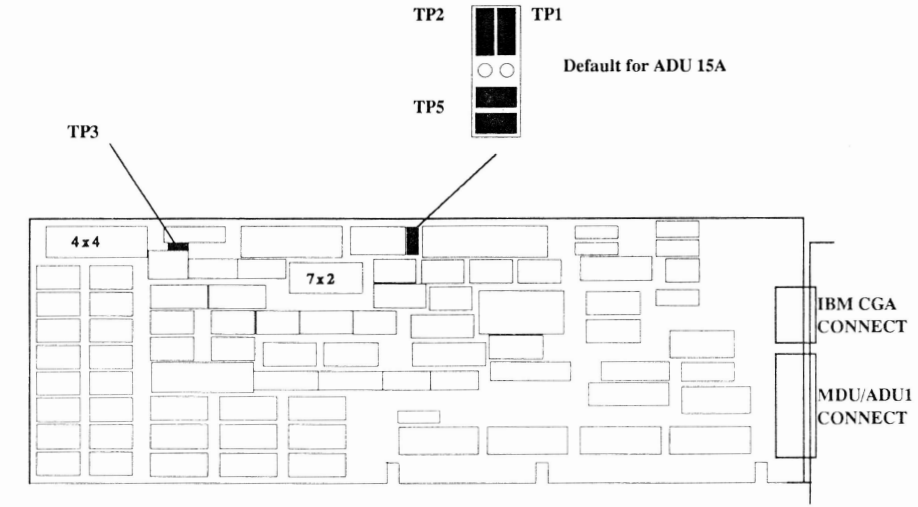
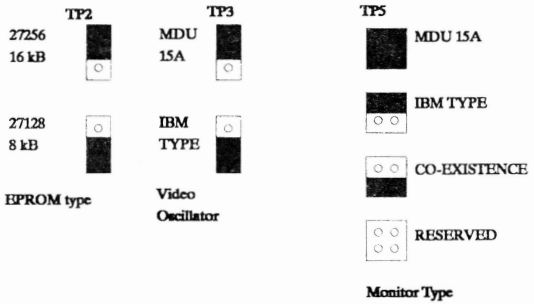
NDC286 JUMPER SETTINGS

THE FOLLOWING JUMPERS ARE LOCATED IN THE NDC286 :

Name	Used for	Default Setting
TP1	Testing	Connected
TP2	EPROM Size	27256
TP3	Monitor Type	MDU15A/ADU15A
TP5	Monitor Type	MDU15A/ADU15A





FIRMWARE VERSION HISTORY ASC/AWS NDC286 DISPLAY CONTROLLER

FW10	NA	27.02.86	First delivered version
FW20	FCO 6047	18.03.86	IC38 729508/A replaced with 729508/B
FW30	FCO 6067	18.03.86	IC 729508/B replaced with 729508/C. Change effect: Softkey handling fixed, display disabled at power-on to eliminate rubbish during IBM/AT power-on.
FW40	FCO 6139	06.06.86	729508/C replaced with new version 729508/D. Effect: Xenix compatibility ensured, 2 new commands added: Active protocol in AT (18) and Get NDC status (17).

OBS: Because of the new size EPROM it will need to change NEW PAL circuit and update hardware.

FW50	FCO 7102	14.10.87	-EPROM FW version has been updated -The Cursor handling and two Fonts in the Font table has been corrected. - 14*8 character set0 Fonts F9H and FAH are now IBM compatible - In the Mode change cursor has been to line 13 : **SOLUTION NEW** Firmware 729508/E

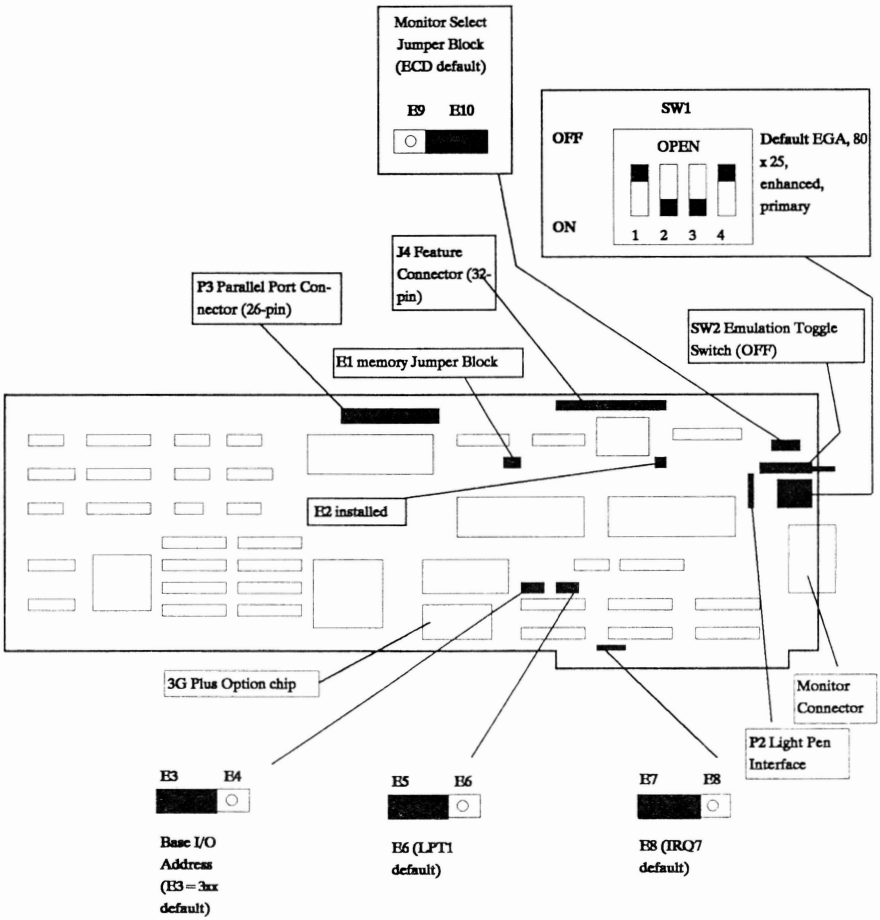
OBS: Because of the new size of EPROM (27256) it will need to change jumpering to position (256).

FW60	FCO 7216	12.10.87	NDC + EGA configuration is enabled. It is possible to use NDC286 with another display controller at the same time by configuring NDC´s jumper connections (TP5 connection 3-4). NDC then emulates IBM monochrome display controller and takes address space B0000H-B7FFFH **: New Firmware 729508/F**
FW70	FCO 7227	27.10.1987	Some fonts were not compatible with DIN standard 66009 **: New Firmware 729508/G**

NDC ROM LIST version 70X

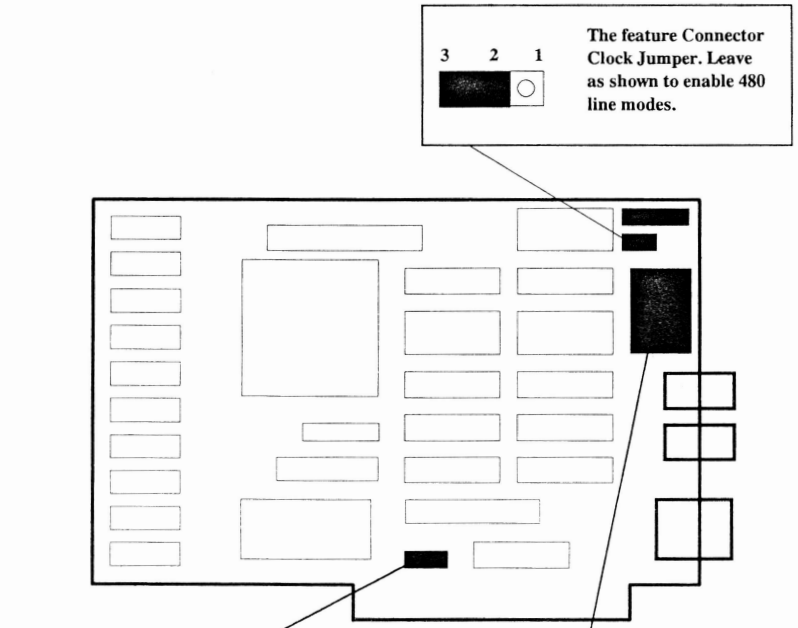
LOC	NAME	COMP. TYPE	MASTER PART NR.	CHECK SUM	NOTES
IC38	FW	27256	729508/G	77D4	EPROM
IC2	DAM	PAL20L8A	729509/B	AD23	PAL
IC5	DEM	PAL16L8	729510/A	43D3	PAL
IC7	DEI	PAL16L8	729511/A	5828	PAL
IC52	DBC	PAL16L8A	729512/A	5C97	PAL
IC55	DIOD	PAL20L8A	729513/A	95C0	PAL
IC72	DMC	PAL16L8	729514/A	16FC	PAL

AST-3G EGA JUMPERING



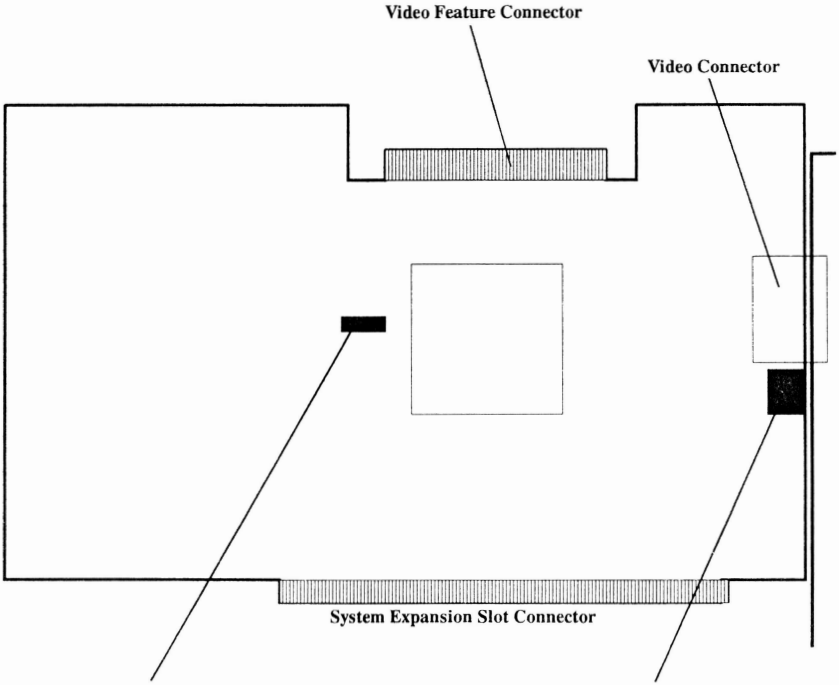
OBS! AST EGA-card does not work with OS/2 operating system.

PARAMETER	DEFAULT	COMMENTS
Card Type, Mode Monitor Primary	EGA 80x25 text ECD monitor Primary SW1-1 OFF, SW1-2 ON, SW1-3 ON, SW1-4 OFF	The SW1 switch block provides the power-up graphics configuration for the AST-3G.
Emulation Toggle Switch	SW2 OFF	This toggle switch is only used with the Plus Option. When ON, it provides CGA software compatibility and HGC/Preview! emulation.
Monitor Type	ECD monitor Plug at jumper block position E10.	This jumper block sets the type of monitor in use. If a monitor other than an ECD is used, move plug to position E9.
AST3-G on-board	Either 64 or 256kB Plug at jumper block position E1 for 256 kB, remove plug for 64 kB	This jumper block shows how much on-board memory your AST3-G has. The default is either 64 or 256 kB. You only need to change the plug if you are upgrading from 64 to 256 kB.
Parallel Port	LPT1 at IRQ7. Plug at LPT jumper block E5 and at IRQ jumper block E8.	This setting indentifies the parallel port and its hardware interrupt number. You may need to change these settings, if there is another parallel port in your PC.
Base I/O Address	3xx Plug at jumper block E3.	The base I/O address is used for PC-to-AST-3G communication. Changing this will destroy software compatibility.



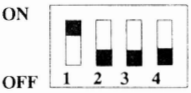
Monitor:	Lever1	Lever2	Lever3	Lever4
Monochrome	OFF	OFF	ON	OFF
Standard RGB	ON	OFF	OFF	ON
(40 column mode is default)				
Standard RGB	OFF	OFF	OFF	ON
(80 column mode is default)				
Enhanced RGB	ON	ON	ON	OFF
(200 line or emulation of standard RGB is default)				
Enhanced RGB	OFF	ON	ON	OFF
(350 line, true enhanced operation is default)				

VGA CARD JUMPERING



W1

Feature
connector
clock Jumper



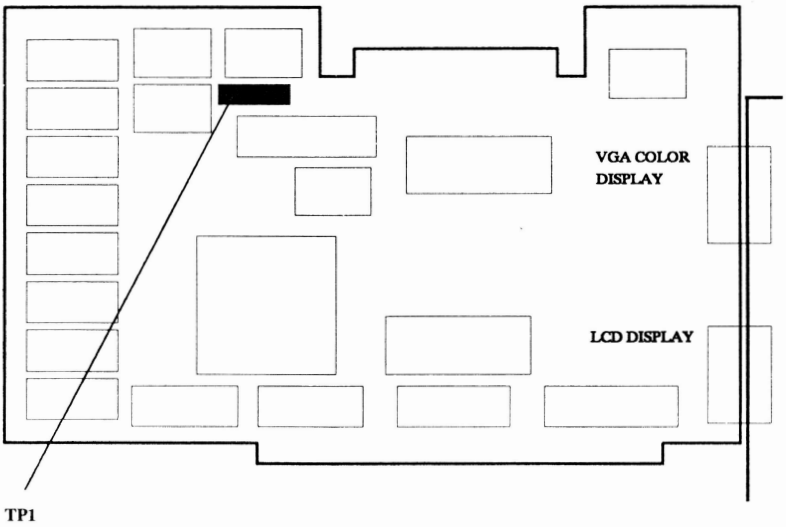
DIP Switch

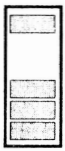
DIP Switch Settings	
Monitor Type	lever1
Standard PS/2 Multi-frequency	OFF ON

Levers 2, 3 and 4 are NOT used and should be set to the OFF position.

Latest BIOS version is 730100A
This version is modified by Nokia.

NVGA CARD JUMPERING



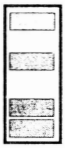


VCLK2 = MCLK

MCLK = 36.000 MHz
VCLK1 = 28.322 MHz
VCLK0 = 25.175 MHz

DEFAULT SETTINGS

VCLK2 = EXTCLK
FEATURE CONN.
MCLK = 36.000 MHz
VCLK1 = 28.322 MHz
VCLK0 = 25.175 MHz



VCLK2 = VCLK1

MCLK = VCLK1

VCLK1 = 28.322 MHz
VCLK0 = 25.175 MHz

FEATURE CONN.
VCLK2 = EXTCLK
MCLK = VCLK1

VCLK1 = 28.322 MHz
VCLK0 = 25.175 MHz

No installation : R13, L1, L2, L4, X4-6, C4, C6, C7, C21, C31

AC40160 NVGA VERSION HISTORY

HW	FCO	DATE	
-	ECO 8067	25.03.1988	Interference on the screen when screen has white background. (black lines on white screen) **SOLUTION:** Resistor C4 has been removed from the board. (This modification has been made in the factory for all boards)
-	ECO 8076	30.03.1988	Interference on screen if white background is used. Big black areas have shadows. **SOLUTION:** C5 has been replaced with a new one. New value for C5 is 4.7nF, code for the capacitor is 2309066 (No boards has been delivered from factory, all boards in the factory have been updated)
-	ECO 8084	21.04.1988	When LDU-11A is used in some certain mode there is some noise in the screen because of the interference in the HOR and VERTICAL signal. **SOLUTION:** The value of resistor R9 and R11 must decrease. **OLD VALUE: 68R1** **NEW VALUE: 33R2**
A	ECO 8109	10.03.1988	**NEW LAYOUT A OF NVGA-BOARD** The new NVGA layout version A may be installed in PC/XT chassis.
FW2	ECO 8217	21.10.1988	**Version notice for NVGA video ROM ver. B** The NVGA VIDOE ROM is a EPROM-component of the NVGA -display controller. The EPROM contains mainly MS-DOS video BIOS routines (INT 10h). The NVGA display controller can drive the flat panel (the LDU 11A) and VGA compatible analog mono and color monitors. Original BIOS source: Paradise 07/14/88

The following objects has been inserted for version B (Checksum 2B00H)

- found bugs has been corrected for
- in the Graphics modes there is no more inverting on the LDU 11A, because so many graphics software packages invert the screen themselves. (e.g. DOS 4 shell, Windows, Ventura)
- backward compatibility (CGA and MGA has been improved for the LDU 11A display unit. Use the NVGA utility to set the video mode.
- it is possible to lock video state when LDU 11A is connected.
- nine-dot fonts are not used, i.e. 16*9 -> 16*8, 14*9 -> as default in any display (ergonomic requirements)
- 350 line modes polarity has been changed for LDU 11A
- the blanking timing has been changed for LDU 11A
- the version character B has been inserted to the EPROM so that the NVGA utility program version 1.4 displays the NVGA video BIOS version

FW3 **ECO 8225** **24.11.1988**

Version notice for NVGA video ROM ver. C

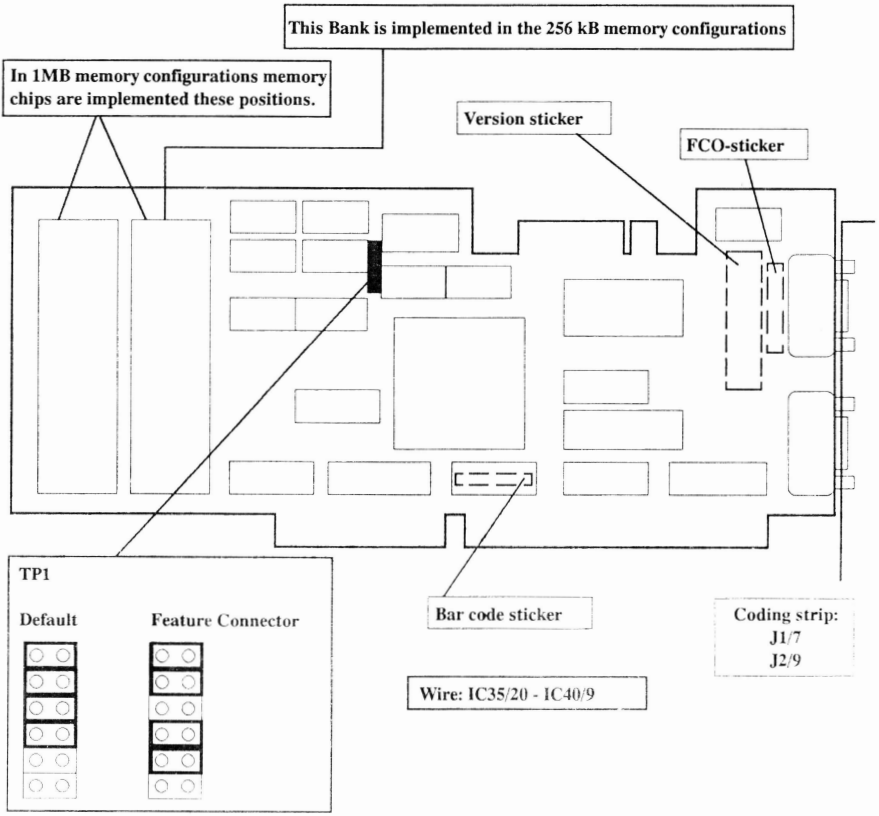
Paintbrush problem
Paintbrush did not work properly on the NVGA board. When mouse is moved it can not return the original color. The reason for the problem was in the mode tables. The correction has been implemented to the video ROM

Modified files
Only file PVGATABL.ASM has been modified after B version. For standard mode tables mode 0, 0*, 0+, 2, 2*, 4 and 1, 1*, 3, 3*, 3+ has different tables as in PARADISE´s video BIOS.

NVGA2

Spare part no: AC 40162.1, 40162.2, 40162.3

256 kB	512 kB	1MB
AC40162.1	AC40162.2	AC40162.3
NOT INSTALLED	**NOT INSTALLED**	**NOT INSTALLED**
R11	R6, 11-12	
RN6		RN6
C4	C4	C4
L1-2, 4	L1-2, 4	L1-2, 4
IC1, 3, 5, 7, 9, 11, 13, 15	IC17-24	IC1-16
IC17-24, 30		IC30
X5-8	X5-8	X5-8



NVGA2 FW -HISTORY
AC40162

ECO NO: H89038 DATE:24.01.1989 HW-, CO, FW2

Reason:
The Identification problem has been corrected.

New FW-Version 730126A ---> 730126C

ECO NO: H89045 DATE:08.02.1989 HW-, CO, FW3

The NVGA2 VIDEO ROM is the EPROM-component of the NVGA2-Display Controller. The EPROM contains mainly MS-DOS video BIOS-routines (INT10H).
The NVGA2 display controller can drive Flat panel (LDU11A), VGA+ monitors and VGA compatible Analog MONO and COLOR Monitors.

The following changes has been made for version C (Checksum 5200).

1. The Bios recognizes different memory configurations in POST- rou tines.
   The refresh problem with 1MB DRAMs has been fixed.

2. The Bit 16 Option has been used. It means Faster Write and Read in Text and linear Graphics modes.

3. For the LDU11A the Graphics modes are not inverted as default.

4. The inverting is possible also in the modes; MDA, CGA and HERCULES

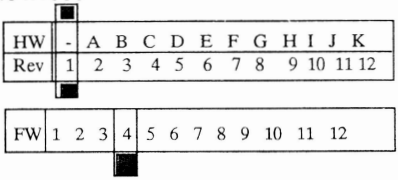
5. The BOLD Fonts 'm' and '0' (zero) has been modified to more readable.

6. The version bytes has been changed; B ---> C

7. The Video BIOS does not change the overscan and DAC lock bits.

8. Problems with Fonts loading in the Mode 56H has been fixed

FCO NO: H89121 DATE:19.04.1989



REASON, MONITOR IDENTIFICATION PROBLEM;

A: - Occasionally Monitor Identification Fails.

- Monitor Identification is Based on Different REFERENCE VOLTAGE At Comparator (CONTROLLED VIA CONNECTOR´s ID-PINS) and Different Load Resistance (COLOR/MONO).

- Are noticed that REFERENCE VOLTAGE´s safety area´s between different Monitor types are too small. Depending on Resistors Dac´s and Supply Voltage´s Accuracy The DAC´s Output in Vorse Case Overlap The MONITOR´s REFERENCE POINT ---> IDENTIFICATION FAILS.

B: SOLUTION:
Change The MONITOR´s REFERNCE POINTS to get BIGGER SAFETY areas Between DIFFERENT MONITOR TYPES.
ALSO BIOS HAVE TO BE MODIFIED (VERSION C --> D)

C: CHANGE THE FOLLOWING COMPONENTS: (NVGA2 PCB "-") !!

	old value	new value	new code
R1	267R	95R3	A1412159
R8	68R1	16R2	A1400339
R9	2K21	681R	A1403891
R10	365R	95R3	A1412159

NOTE: BOTH BIOS AND RESISTOR´s MUST BE CHANGED AT THE SAME TIME*

*** ALL FUTURE BIOS VERSIONS WILL REGUIRE THESE NEW RESISTOR VALUES.**

FCO NO: H89148 DATE:19.05.1989

HW	-	A	B	C	D	E	F	G	H	I	J	K
Rev	1	2	3	4	5	6	7	8	9	10	11	12

FW	1	2	3	4	5	6	7	8	9	10	11	12

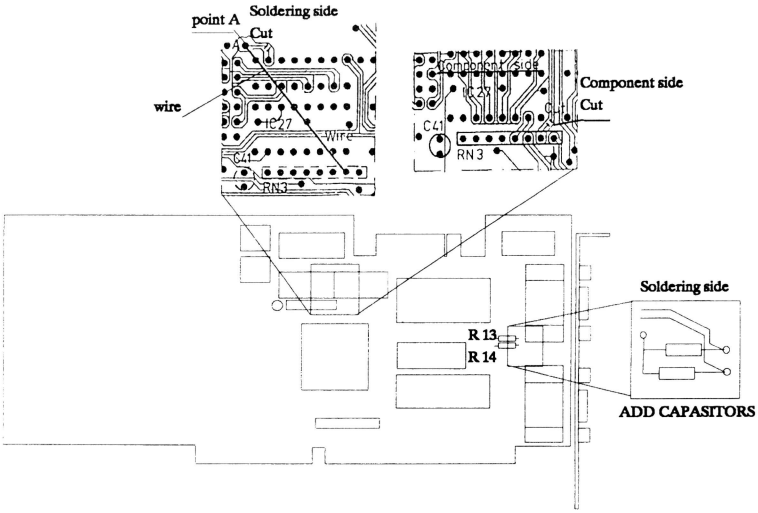
REASON, TO GET NVGA2 FULLFILL OUR RFI REQUIREMENTS;

A: NVGA2 Card does not fullfill RFI specifications

B: SOLUTION:

	Old value	New value	New code
R7	33R2	Single ferrite bread (A3602746)	
R20	47R5	---------- || ----------	

Insert 47 pF capasitors (code A2309034)
to Hsync and Vsync signals. (soldering side)



Wire :
IC 35/pin 20 - IC 40/pin 9 (component side)
RN 3/7 - point A (soldering side)

Cut :
IC 33/pin 35 - P3B/pin 4 (ss)
IC 25/2 (ss)
RN3/7 (cs)

FCO NO: H89178 DATE:26.06.89

HW	-	A	B	C	D	E	F	G	H	I	J	K
REV	1	2	3	4	5	6	7	8	9	10	11	12

FW	1	2	3	4	5	6	7	8	9	10	11	12

A, PROBLEM, B SOLUTION, C, IMPLEMENTATION

A. PROBLEMS ; POSITIVE MODE COLOURS/GREY SCALE:
- DU146: INCOMPATIBLE COLOURS (ONLY 8 COLOURS AVAILABLE)
- DU151: ILLOGICAL WAY OF CALCULATING THE GREY SCALE (ONLY 8 SHADES)

MANIPULATING THE COLOR DAC CAUSED PROBLEMS IN OS/2 AND ALSO IN DOS WHEN RUNNING BIND BASED PROGRAMS.

B. **BIOS VERSION E**

ROM BIOS DATED: 06/06/1989
EPROM CHECKSUM 1600H

MODIFICATIONS (D -->E)

POSITIVE MODE COLOURS/GREY SCALE COMPLETELY RESEIGNED:
- **DU146:** 16 COMPATIBLE COLOURS- ONLY WHITE, BLACK, GREY AND INTENSIFIED WHITE MODIFIED ("ROTATED")

- **DU151:** 16 LEVEL GREY SCALE BASED ON THE COMPATIBLE (NEGATIVE MODE) SCALE

- COLOUR DAC NO LONGER MANIPULATED; THE POSITIVE IMAGE IS PRODUCED BY MODIFYING THE EGA PALETTE REGISTERS.

- DEFAULT OPERATION AFTER BOOT-UP:
  - **DU146**: NEGATIVE IMAGE
  - **DU151**: POSITIVE IMAGE

- THE VERSION SPECIFIER CHARACTER AT THE ROM OFFSET 72H HAS BEEN UPDATED ("D --> E")

- THE ROM BIOS NOW CONTAINS A POINTER TO THE SPECIAL NOKIA STATUS BYTE.
  THE POINTER CAN BE FOUND AT THE ROM OFFSET 7AH.

C. ADD DISKETTE "NVGA UTILITY AND ERGONOMIC UTILITIES" AND INSTRUCTION "NVGA UTILITIES (JUNE 20TH 89)" SHOULD BE ADDED TO THE PC PACKAGE WHEN DOS IS INSTALLED.

FCO NO: H89188 DATE:06.07.1989

HW	-	A	B	C	D	E	F	G	H	I	J	K
REV.	1	2	3	4	5	6	7	8	9	10	11	12

FW	1	2	3	4	5	6	7	8	9	10	11	12
						■						

A. PROBLEM B. SOLUTION C. IMPLEMENTATION

A: PROBLEM

1. BIOS VERSION E BOOTS UP A MONOCROME MONITOR (DU151 OR STANDARD) IN COLOR MODE (BIOS MODE 03H). THIS CAUSES OS/2 TO INCORRECTLY ASSUME A COLOR MONITOR WHICH IN TURN CAUSES ERRORNEOUS BEHAVIOUR IN THE COLOR SETUP PROCEDURES.

2. SOME APPLICATIONS (E.G. NORTON UTILITY NCC.EXE) CANNOT CHANGE THE OVERSCAN (BORDER) COLOR IN DU146/DU151 ENHANCED MODE EVEN WHEN THEY EXPLICITELY WANT TO DO SO BECAUSEOF "LOCK" IN A PARTICULAR BIOS CALL (0BH, SET COLOR PALETTE).

B. SOLUTIONS:

1. BOOT-UP CONDITIONS CHANGED:
   - MONOCHROME MONITOR: DEFAULT VIDEO MODE IS 07H (MONO)
   - COLOR MONITOR: DEFAULT VIDEO MODE IS 03H (COLOR)

2. "LOCK" REMOVED

UPGRADEABILITY OF DELIVERED UNITS:

	UPGRADEABILITY
BIOS CHANGE FROM "D" OR "E" TO "F"	FULL
BIOS CHANGE FROM "A", "B", "C" TO "F"	LIMITED

NOTE: CHANGE ORDER NVGA2 NO: H89121
DT3X6 NO: H89122

MODIFICATIONS (VERS E ---> F)
DATE: 07/07/1989
CHECKSUM: FE00H

FCO NO: H89164 DATE:06.06.1989

HW	-	A	B	C	D	E	F	G	H	I	J	K
Rev	1	2	3	4	5	6	7	8	9	10	11	12

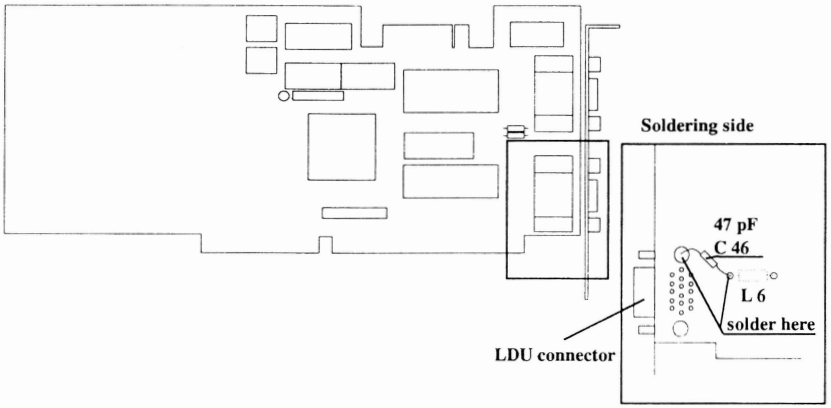
NVGA2 DOES NOT WORK PROPERLY WITH LDU 11A

A: PROBLEM: DOTCLK harmonics radiates when LDU 11A is used exceeding CISPR limit.

B: SOLUTION: Add 47 pF ceramic capasitor in the DOTCLK signal.

C: IMPLEMENTATION:

Add 47 pF cer capasitor to the solder side of the pcp, see picture below.



ECO NO: H90031 DATE: 15.02.1990
UNIT: NVGA2
UNIT CODE: AC40162.1
AC40162.2
AC40162.3

HW	-	A	B	C	D	E	F	G	H	I	J	K
Rev.	1	2	3	4	5	6	7	8	9	10	11	12

FW	1	2	3	4	5	6	7	8	9	10	11	12

STATEMENT: REASON FOR CHANGE A, PROBLEM B, SOLUTION C, IMPLEMENTATION .

A. TO KEEP SUPPORTED VGA BIOS VERSIONS AS SMALL AS POSSIBLE WE GIVE UP BIOS PAGING MECHANISM AND MAKE THE NEXT BIOS VERSION (730126G) LINEARY ADDRESSING.

B. PAL CHIP WHICH CONTROL PAGING MECHANISM HAVE TO CHANGE.

C. THE PAL CHIP HAS TO CHANGE (MUST!) AT THE SAME TIME WITH BIOS IN ORDER FOR THE NEW BIOS VERSION TO WORK. (BIOS VERSION 730126G)

PAL CHIP:	IC38	730050A = > B CS: 2B71
BIOS CODE:	IC36	730126A = > G CS: 4000

A: Problem

1. Any former versions did not recognize the ESA standard video mode numbers 6Ah and 6Bh. The code only new about modes 58h, 59h, 800x600 pixels graphics modes (16 colour and monochrome).

   The latest version from Paradise (Western Digital), version 018, Dec 20, 1989, recognizes the new modes but fails to correctly test for them at a few places.

2. BIOS version F had the overscan "lock" in call 0Bh removed to allow some applications (e.g. Norton utility NCC.EXE) change the overscan (border) color in DU146/DU151 enhanced mode.

   This had the inconvenient side effect that the DOS CLS command managed to turn the border black unexpedtedly. This happened most often in mode 3 with positive image (i.e. white back ground).

3. There are synchronizin problems with some (older) monitors in the Optimo modes (10 sync pulses are not sufficient).

4. Former BIOS versions used the 8 pixel wide text fonts even in modes providing a 9 pixel wide character cell.

B: Solutions

1. This version is build on top a new BIOS release from Paradise systems (Westerm Digital) with support for new mode numbers:

6A:	800 x 600	16 colours
6B:	800 x 600	monochrome

   Modules PVGABCO9 and PVGABCCD have been corrected to properly test for the new modes.

2. Overscan lock partially reinstalled. Application programs can change the overscan using BIOS call 0Bh in negative image (black background) mode only.

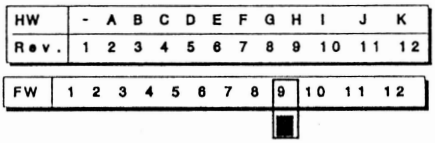
3. Twelve (12) sync pulses are now generated for the VGA + (Optimo) modes. The IBM COMPatible modes are unaffected, naturally.

4. BIOS now uses true 9 pixel wide fornts (9x16 or 9x14) when possible (never on the LDU 11A).

NOTE !!

Construction of the BIOS ROM chip now assumes linear non-paged memory mapping (a PAL change, pages 6 and 7 no longer swapped), BIOS ROMs for old and new NVGA2 cards are thus not directly interchangeable.

FCO NO: H91014 DATE: 30.01.1991
UNIT: NVGA2
UNIT CODE: AC40162.1
AC40162.2
AC40162.3



STATEMENT: REASON FOR CHANGE
A. PROBLEM
B. SOLUTION
C. IMPLEMENTATION .

A1. BIOS Call 00, Function 7F, Subfunction 02: MORE STATUS fails to report the correct memory-size if 256K in standard mapping. Returns 0. should return 4 (4x64K = 256K). If 256 in Paradise mapping, BIOS returns correct values and this is the normal situation. Problem is only visible when an external program resets or remaps memory mapping.

A2. Monitor recognition fails on some machines. The monitor-detect routine is only syncronized to vertical retrace when sampling video-level. Can hit horizontal blanking and fail.

B1, 2. BIOS code corrected.

C1, 2. Change VGA BIOS version 730126H = > 730126J
Checksum: 4D00
Date: 901010

Modifications from version H to J.

Automatic Monitor Detection has been corrected.

INT 10, BIOS Call 00h, Function 7Fh, Subfunction 02h is corrected to return the correct memory-size if 256K in standard mapping. Now returns 4 (4x64K = 256K).

The version specifier character at the ROM offset 72h has been updated H = > J. Please note that version I is not released, since it could be confused with the NVGA2i project.

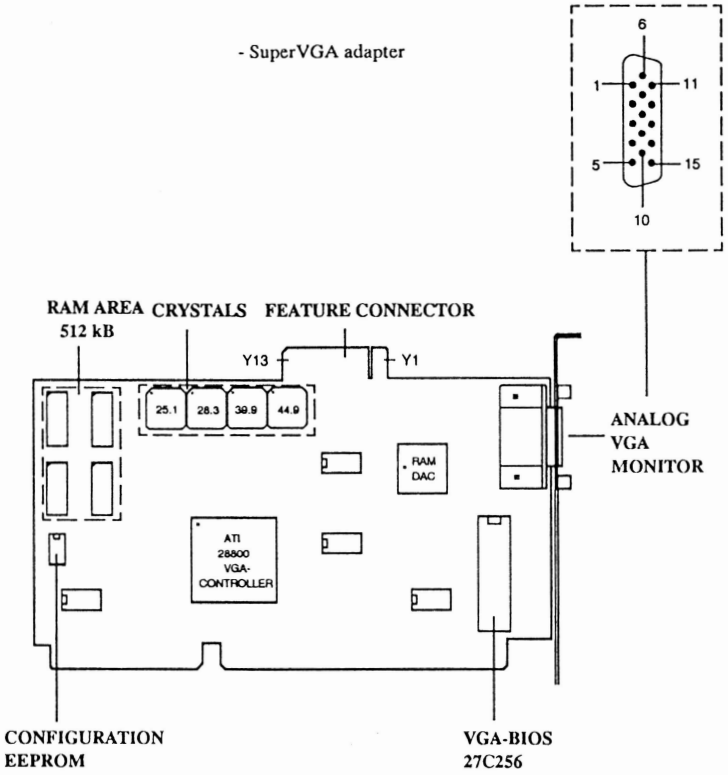
The date-string at ROM offset 0Ah is updated 10/10/90 12:00:00.

EPROM LIST AC40162 15.06.1990

LocName	Comp Type	Comp Code	Master Part NO:	Check Sum	Notes
IC40 EPROM	27256-20	A4327092	730126H 730126J	4900 4D00	900505 901010
IC35 PAL	P20L8	A4329205	730049A	37DE	
IC38 PAL	P20L8	A4329205	730050B	2B71	

NVGA2i, AC40163.2

- SuperVGA adapter



NOTE I

THERE ARE NO JUMPERS ON THE NVGA2i BOARD

THE BOARD CAN BE USED IN 8- AND 16-BIT SLOTS (AUTODETECTION)
IF NVGA2i IS USED WITH ANOTHER ADAPTER (HERC, MDA OR CGA)
NVGAI HAS TO BE USED IN 8-BIT SLOT

IF MONITOR WILL BE CHANGED, BEFORE CHANGE
IF NVGA2i IS CHANGED, AFTER CHANGE
— TYPE:

SUPERVGA DEFAULT ENTER

SUPERVGA-FILE CAN BE FOUND FROM:
NOKIA SUPER-VGA UTILITIES AND DRIVERS DISK (ASRD06425E)

Display connector:

Monitor-connector is a 15-pole female AMP connector. Pin-assignments are as follows:

Pin	Signal name:
1	Red
2	Green
3	Blue
4	ID 2
5	(reserved, digital ground)
6	Red Return
7	Green Return
8	Blue Return
9	Key
10	Sync Return (digital ground)
11	ID O
12	ID 1
13	Horizontal Sync
14	Vertical Sync
15	(reserved)

Video Feature Connector:

Note: All feature connector signals are TTL levels.

Pins from Y1 to Y13 locate component side. Pins form Z1 to Z13 locate solder side.

Pin:	Name:	Description:	Pin:	Name:	Description:
Yl	PDO	Pixel Data O	Z1	GND	
Y2	PDl	Pixel Data 1	Z2	GND	
Y3	PD2	Pixel Data 2	Z3	GND	
Y4	PD3	Pixel Data 3	Z4	EPDATA	Enable pixel data
Y5	PD4	Pixel Data 4	Z5	ESYNC	Enable sync signals
Y6	PD5	Pixel Data 5	Z6	EPCLK	Enable pixel clock
Y7	PD6	Pixel Data 6	Z7	NC.	
Y8	PD7	Pixel Data 7	Z8	GND	
Y9	DCLK	Pixel clock	Z9	GND	
Y10	BLK	BLANK	Z10	GND	
Yll	HSY	Horizontal sync	Z11	GND	
Y12	VSY	Vertical sync			
Y13	GND				
Z13	NC.				

NVGA2i BOARD (AC40163.2) FW Vers. HISTORY

LOC.	NAME	COMP	NOKIA CODE	PART N:o	CS	Ver N:o	DATE	FW
IC17	BIOS	27C256-20	A4327008	A730357B	FE00	B	910110	2
				A730357C	0500	C		3
				A730357D	0500	D	910214	4

NVGA2i FW AND HW VERSION HISTORY

FCO NO: H91005
DATE: 910125

HW	- A B C D E F G H I J K
Rew.	1 2 3 4 5 6 7 8 9 10 11 12

FW	1 2 3 4 5 6 7 8 9 10 11 12

STATEMENT: A PROBLEM, B SOLUTION, C IMPLEMENTATION

A. WRONG COLORS WHEN USING DU146 IN MONO MODE

B. BIOS FAULT FIXED

C. REPLACE BIOS 730357B TO 730357C

FCO NO:	H91032
DATE:	910214

HW	- A B C D E F G H I J K
Rew.	1 2 3 4 5 6 7 8 9 10 11 12

FW	1 2 3 4 5 6 7 8 9 10 11 12

STATEMENT: A PROBLEM, B SOLUTION, C IMPLEMENTATION

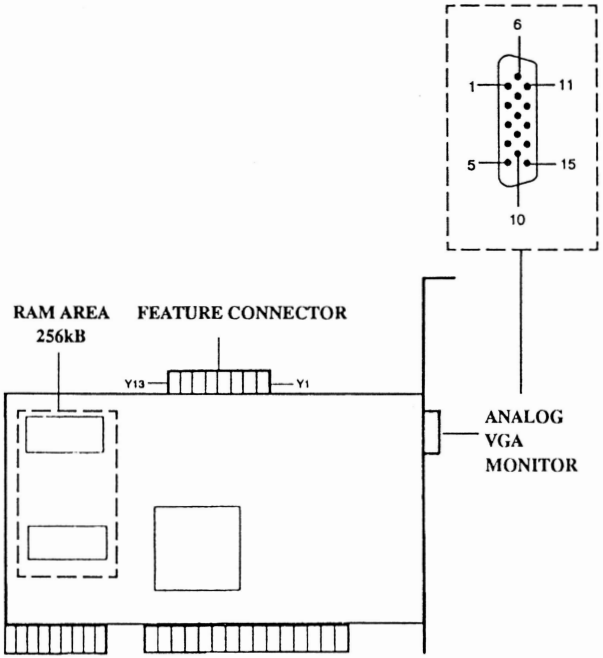
A. BUG IN BIOS CALL 1B

B. FIXED A BUG IN BIOS CALL 1B. STATUS IN MISC STATE (OFFSET 2D) WAS PICKUP FROM THE WRONG PLACE AND STATUS OF THE GRAYSCALE WAS MISSING. AFFECTED OPERATION OF MODE.COM INDOS3.30 WITH MONOCHROME MONITOR.

ADDED A 'SOFT LOCK' TO BIOS CALL 10 FUNCTION 2. OVERSCAN REGISTER IS NOT RELOADED IF NOKIA OPTIMO FEATURES ARE ENABLED AND IN GRAPHICS MODES OR IN INVERTED TEXT MODES. WINDOWS 3 RELOADED A BLACK OVERSCAN WHICH NOW IS FIXED. OVERSCAN COLOR REMAINS WHEN STARTING WINDOWS. BIOS CALL 0B HAS THE SAME TYPE OF 'SOFT LOCK'. THIS IS COMPATIBLE WITH NVGA2.

C. REPLACE BIOS 730357C TO 730357D

NVGAI (AF34027)



NOTE !

THERE ARE NO JUMPERS ON THE NVGAi BOARD

THE BOARD CAN BE USED IN 8- AND 16-BIT SLOTS (AUTODETECTION)

Display connector:

Monitor-connector is a 15-pole female AMP connector.
Pin-assignments are as follows:

Pin	Signal
1	Red
2	Green
3	Blue
4	ID 2
5	(reserved, digital ground)
6	Red Return
7	Green Return
8	Blue Return
9	Key
10	Sync RetuRN (digital ground)
11	ID 0
12	ID 1
13	Horizontal Sync
14	Vertical Sync
15	(reserved)

Video Feature Connector:

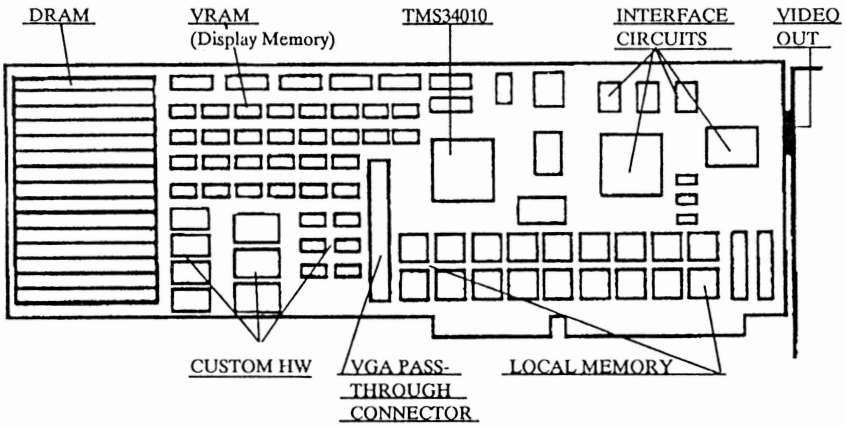
Note: All feature connector signals are TTL levels.

Pins from Y1 to Y13 locate component side. Pins form Z1 to Z13 locate solder side.

Pin	Name	Description	Pin	Name	Description
Y1	PD0	Pixel Data 0	Z1	GND	
Y2	PDl	Pixel Data 1	Z2	GND	
Y3	PD2	Pixel Data 2	Z3	GND	
Y4	PD3	Pixel Data 3	Z4	EPDATA	Enable pixel data
Y5	PD4	Pixel Data 4	Z5	ESYNC	Enable sync signals
Y6	PD5	Pixel Data 5	Z6	EPCLK	Enable pixel clock
Y7	PD6	Pixel Data 6	Z7	NC.	
Y8	PD7	Pixel Data 7	Z8	GND	
Y9	DCLK	Pixel clock	Z9	GND	
Y10	BLK	BLANK	Z10	GND	
Yll	HSY	Horizontal sync	Z11	GND	
Y12	VSY	Vertical sync	Z12	NC.	
Y13	GND				
Z13	NC.				

NOKIA GRAPHICS ADAPTER 1024

AF34025



NOTE ! There are no jumpers on the 1024 board.

Resolutions: 640x480 with 16 colours, non interlaced
800x600 with 16 colours, non interlaced
1024x768 with 16 colours, interlaced or non interlaced

Monitor Support:	DU146, DU151	800x600, non interlaced, 70Hz 1024x768, interlaced, 43.5 Hz
	SALORA 445G	800x600, non interlaced, 77.3 Hz 1024x768, non interlaced, 74.6 Hz

Video Specifications: Video level are analog with optional composite sync-on-green.
Video is 0.7 volts p-p, with an optional sync tip of 0.3 volts on green.
No blanking level is provided.
TTL level syncs are provided.

Video connector is a fifteen pin subminiature D-connector to send analog RGB and TTL horizontal and vertical syncs to the monitor.

PIN	SIGNAL	LEVEL
1	red	analog
2	green	analog
3	blue	analog
4	ground	digital
5	ground	digital
6	red ground	analog
7	green ground	analog
8	blue ground	analog
9	N/C	
10	ground	digital
11	ground	digital
12	N/C	
13	H-sync	TTL
14	V-sync	TTL
15	N/C	

N/C = No connection

Delivery package and options:

AF34025	Adapter board (512KB ---> 16 colours) VGA terminator plug VGA pass through cable for std. VGA feature adapter SW on 3.5" diskette (DGIS, GSS**CGI, PM, AI, XDGIS, ACAD) Test pictures for 800x600 and 1024x768 resolutions
ACO9500.296	VGA pass through cable for backplane VGA -connector.